(12) UK Patent Application (19) GB (11) 2 344 436 (13) A

(43) Date of A Publication 07.06.2000

(21) Application No 9927301.3

(22) Date of Filing 18.11.1999

(30) Priority Data
(31) 10328080 (32) 18.11.1998 (33) JP

(71) Applicant(s)
NEC Corporation
(Incorporated in Japan)
7-1 Shiba 5-chome, Minato-ku, Tokyo 108-8001, Japan

(72) Inventor(s)
Keiichiro Tounai

(74) Agent and/or Address for Service
John Orchard & Co
Staple Inn Buildings North, High Holborn, LONDON,
WC1V 7PZ, United Kingdom

(51) INT CL[7]
G03F 1/14

(52) UK CL (Edition R)
G2X XNB

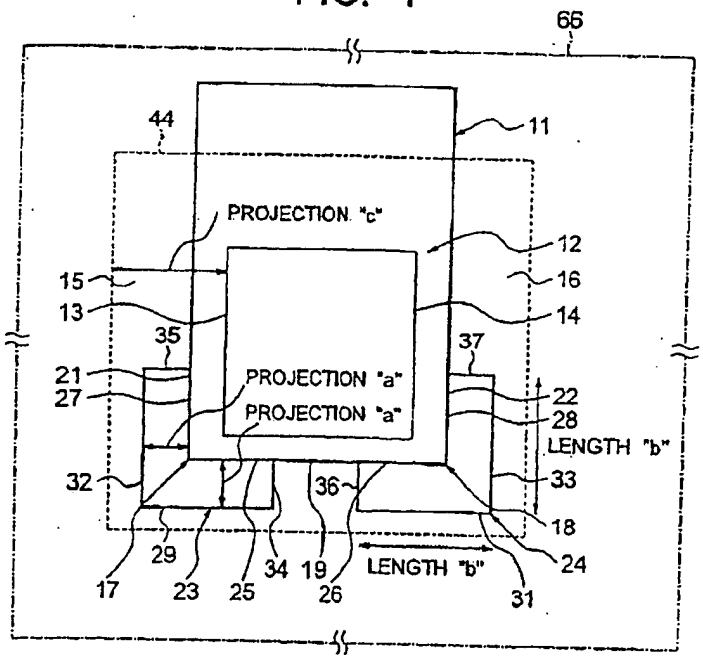
(56) Documents Cited
WO 97/45772 A1 US 5804339 A US 5208124 A

(58) Field of Search
UK CL (Edition R) G2X XNB
INT CL[7] G03F 1/14

(54) Abstract Title
Method of manufacture of a semiconductor device

(57) A method of manufacture of a semiconductor device includes the steps of designating a first peripheral region (44) surrounding a first layer (12); locating at least a corner (17 and 18) of a second layer (11) belonging to the first peripheral region (44); forming a second peripheral region (23 and 24) surrounding the corner (17 and 18); and adding the second peripheral region (23 and 24) to the first layer (12). The method minimises the amount of the data and of the period of time required for correcting any photo-contiguous effect as well as the deterioration of resolution.

FIG. 4



GB 2 344 436 A

FIG. 1

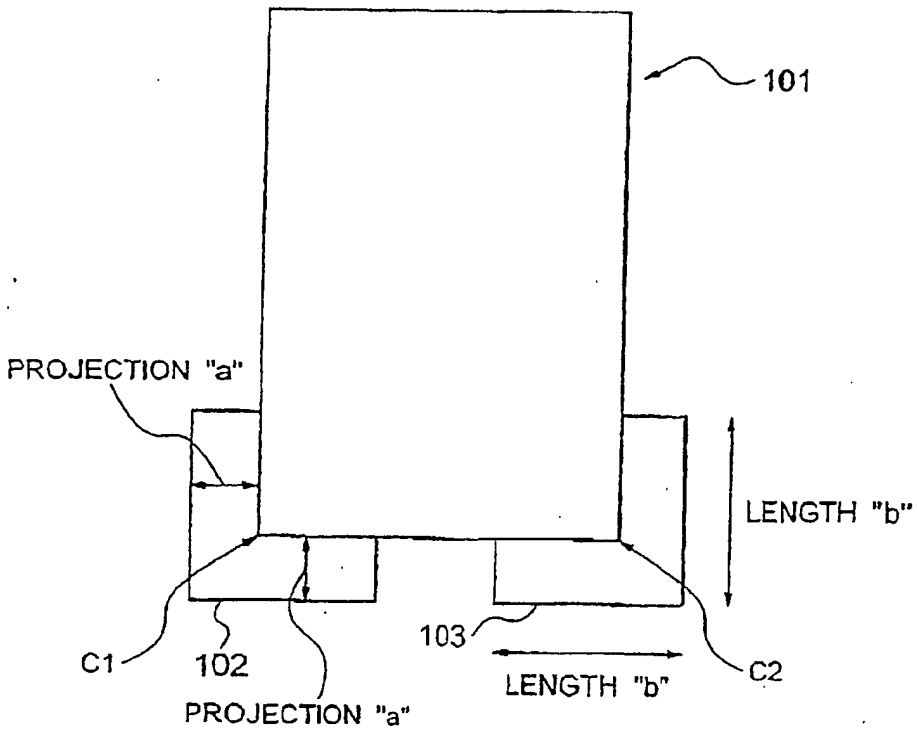


FIG. 2

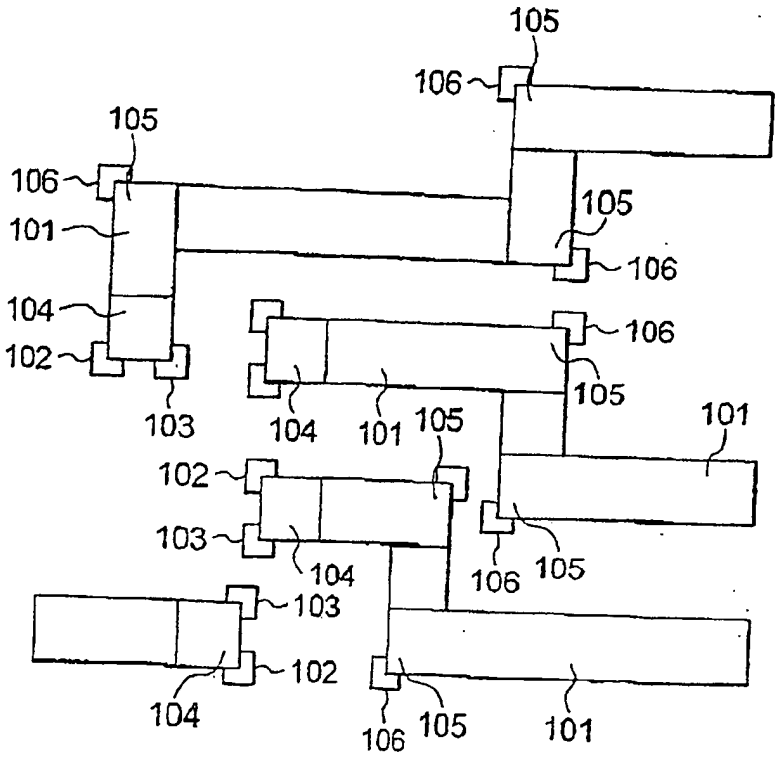

105
106
105
106
101
105
106
104
102
106
105
103
104
101
105
101
102
105
103
104
106
105
103
102
104
106
105
101

FIG. 3

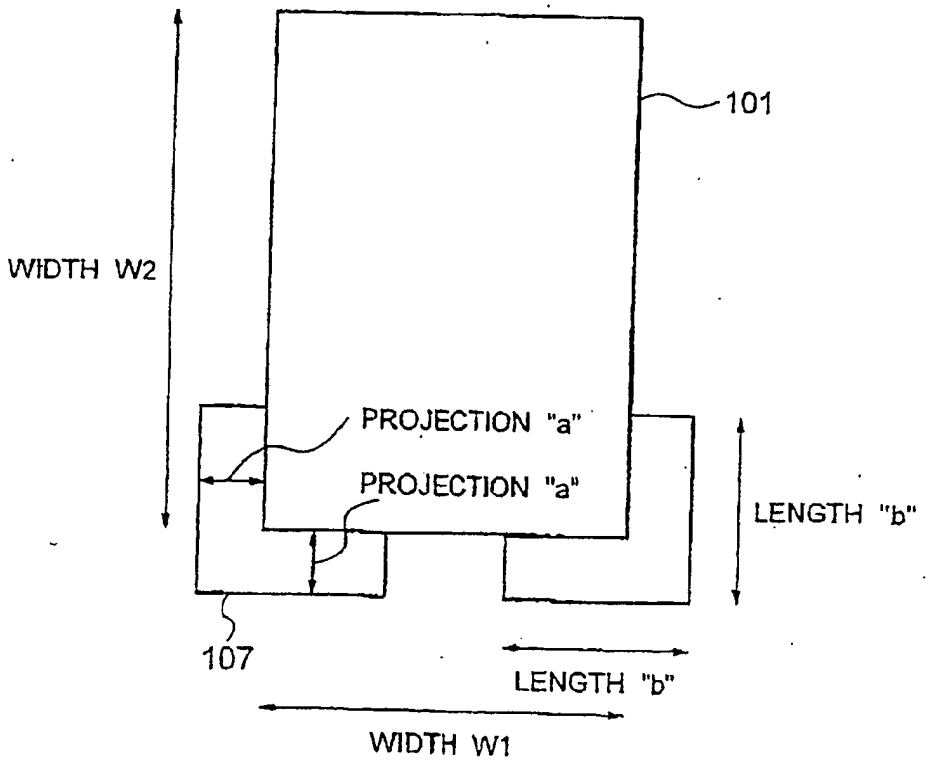

101
WIDTH W2
PROJECTION "a"
PROJECTION "a"
LENGTH "b"
107
LENGTH "b"
WIDTH W1

FIG. 4

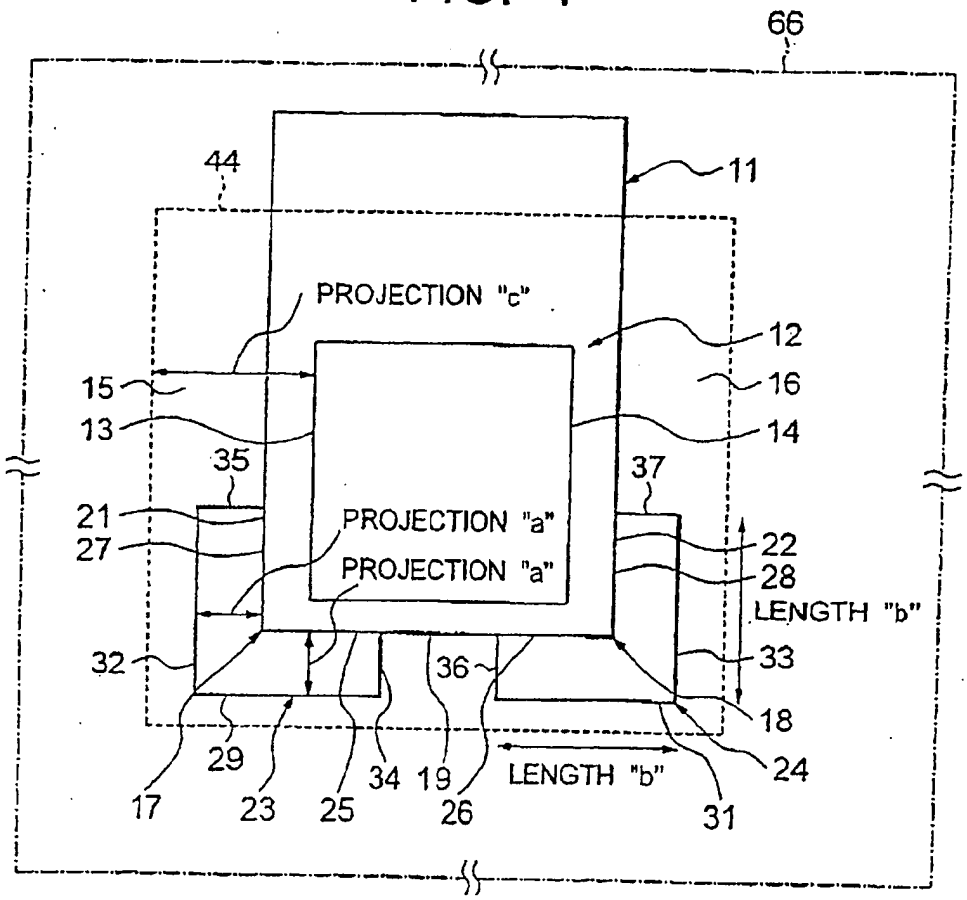

66
44
11
PROJECTION "c"
12
15
16
13
14
35
37
21
PROJECTION "a"
22
27
PROJECTION "a"
28
LENGTH "b"
32
36
33
18
29
24
17
23
25
34
19
26
LENGTH "b"
31

FIG. 5

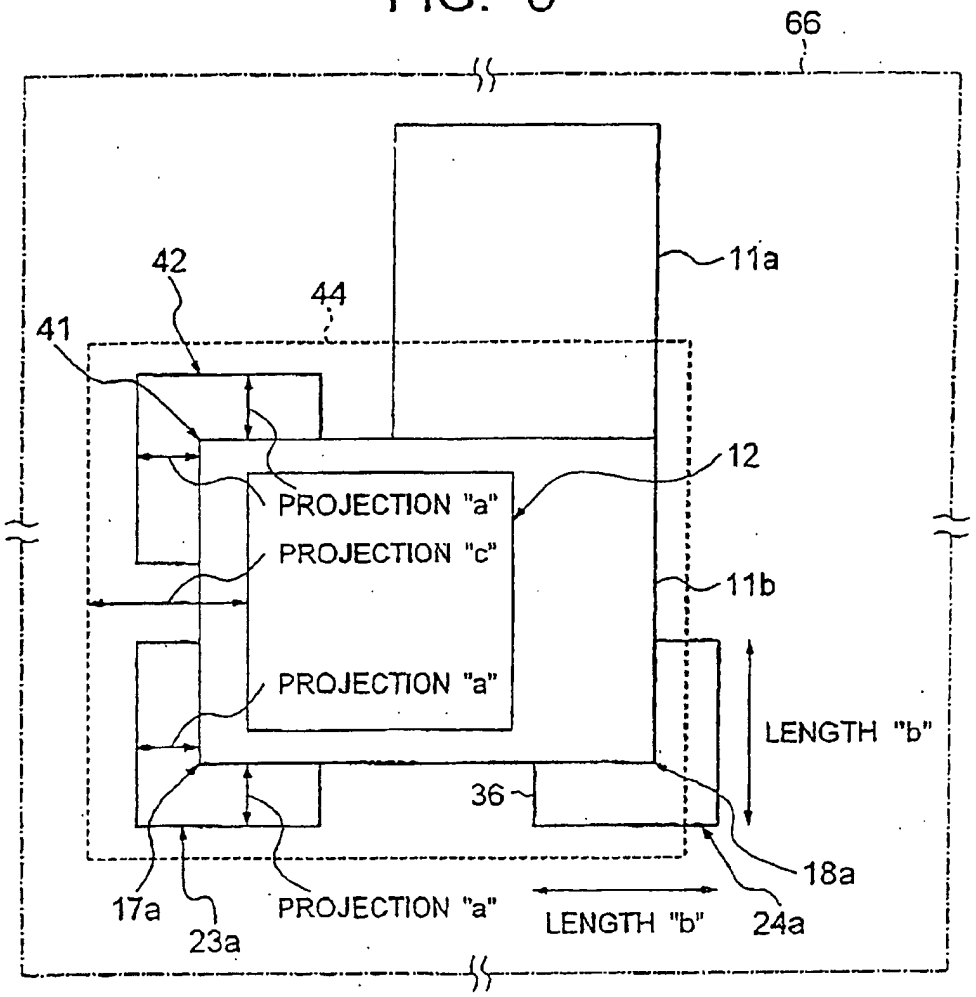


FIG. 6

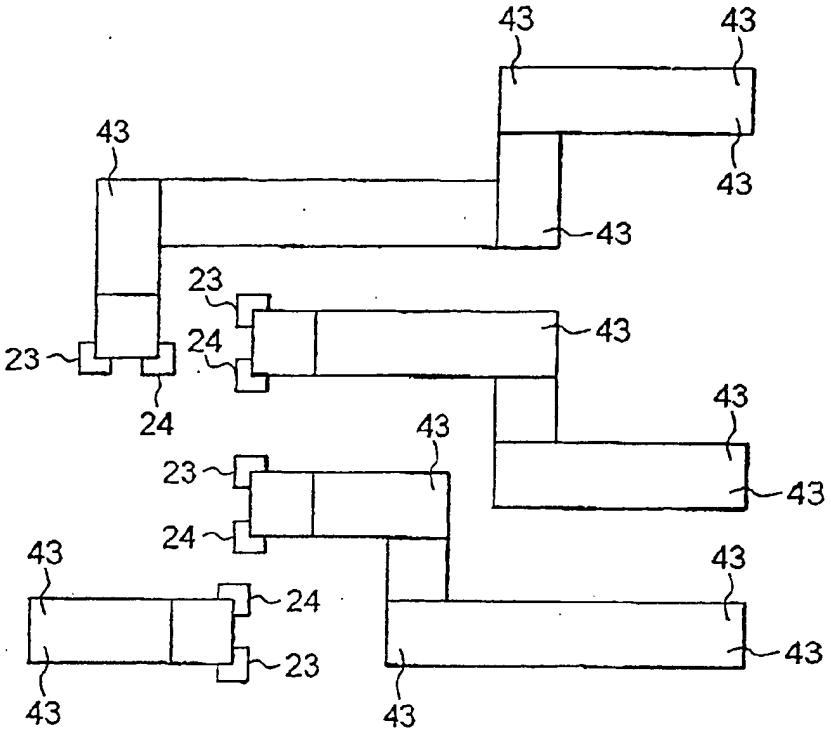


FIG. 7

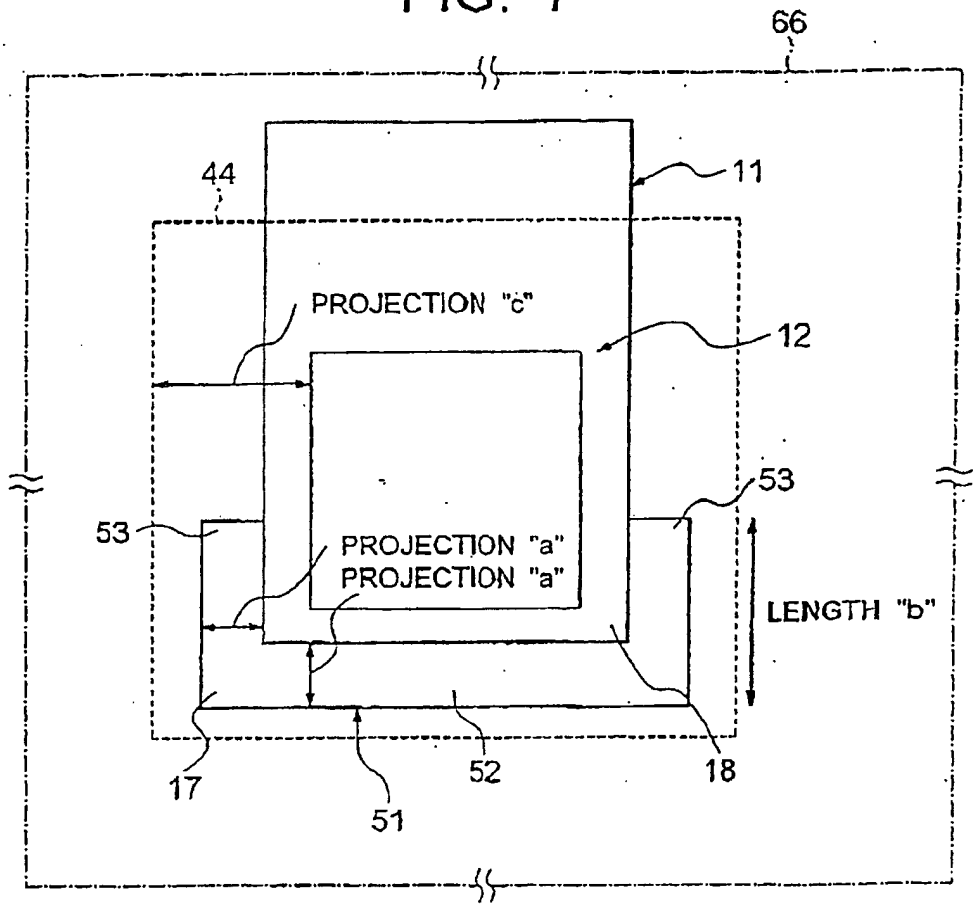


FIG. 8

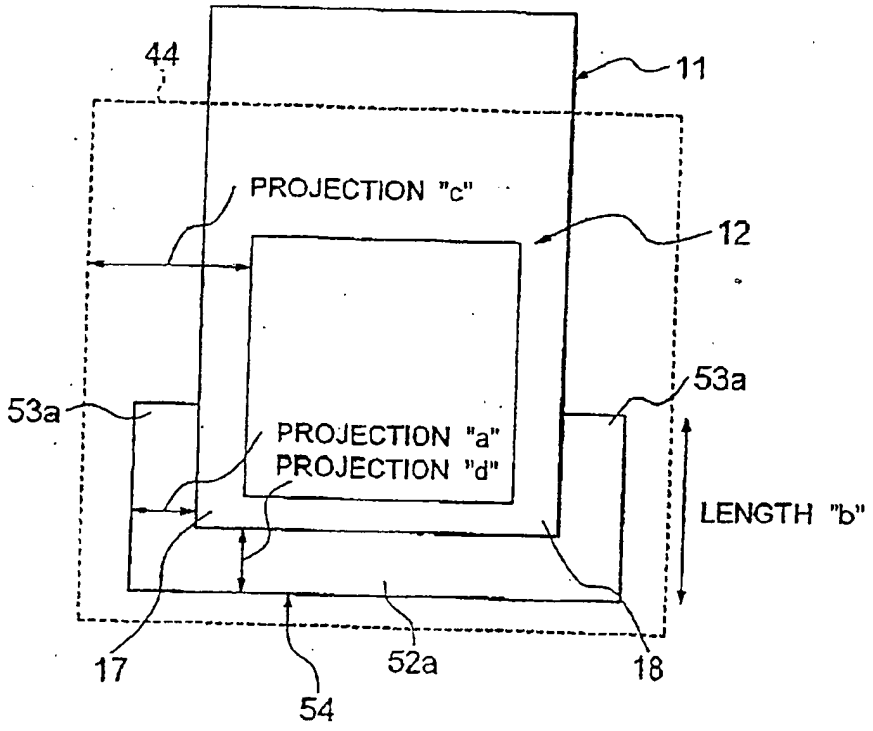
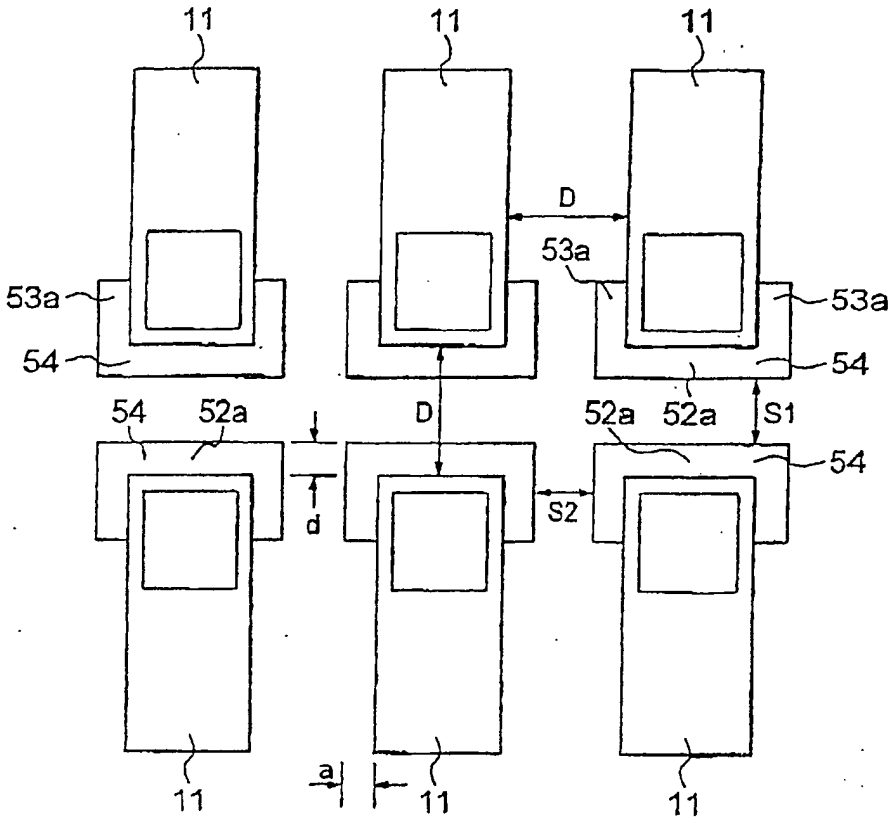

44
11
PROJECTION "c"
12
53a
53a
PROJECTION "a"
PROJECTION "d"
LENGTH "b"
17
52a
18
54

FIG. 9



METHOD OF MANUFACTURE OF A SEMICONDUCTOR DEVICE

The present invention relates to a method of manufacture of a semiconductor device. A method of manufacture of a semiconductor device to be described below, by way of example in illustration of the invention, provides for the correction of any photo-contiguous effect, which prevents the undesired reduction of a length of a pattern at a node where two layers are electrically connected.

In a photolithographic step used in a previously proposed process for manufacturing a semiconductor device having miniaturized patterns, a photo-contiguous effect may occur which results in an inaccurate transfer of a pattern due to photo-interference generated between rays contiguous with each other during an exposure step and a transfer step. A reduction in pattern size error generated as a result of the photo-contiguous effect is required. Pattern size error can be reduced by correcting the photo-contiguous effect in the way described in Japanese patent application 5(1993)-80486. The correction is carried out by modifying the projection of a pattern to be corrected by means of a calculation technique as described in the specification of Japanese patent number 2616467.

When a line end in a circuit pattern, such as an interconnect pattern and a gate pattern, is connected to a connection node, such as a plug and a via hole, a problem arises in that the line end of the interconnect or the gate is reduced in length due to the photo-contiguous effect with the result that

there is a decrease in the connection area down to smaller size than the designed area, resulting in a possible connection deficiency.

Reference will now be made to Figs. 1 to 3 of the accompanying drawings in which:

Fig. 1 is a schematic top plan view for use in describing a previously proposed method for correcting a photo-contiguous effect during the manufacture of a semiconductor device,

Fig. 2 is a schematic top plan view showing the layout of patterns to which the method of Fig. 1 may be applied, and

Fig. 3 is a schematic top plan view for use in describing another previously proposed method for correcting the photo-contiguous effect.

In the previously proposed technique to be described with reference to Figs. 1 and 2, a pair of additional patterns 102 and 103 having a projection "a" and a length "b" are provided at respective corners Cl and C2, of the end of an interconnect 101 in an interconnect pattern.

The projection "a" means the amount of projection of the side of the additional pattern with respect to the side of the corresponding side of the interconnect.

Such additional patterns 102 and 103 are also reduced due to the contiguous effect in order that the interconnect 101 shall have an overall shape complying with the original design.

In the previously proposed technique as may be seen from Fig. 2, an additional pattern 106 is also provided to each bend of non-connection node 105 having one free corner, in addition to the connection nodes 104 having

plugs and two adjacent free corners. This modification or correction is also applied to the nodes where the modification is unnecessary. The technique for making the modification regardless of the existence of the plug significantly increases the size of the mask pattern data due to an increase in the number of figures of the additional patterns. Further, an additional pattern having the same length of projection is added regardless of the length of the side of the connection nodes 104, increasing the amount of modification for the shorter side of the pattern to cause a deterioration in the resolution at the shorter side.

Fig. 3 shows another previously proposed technique for correcting the photo-contiguous effect in connection with the length of the side. The technique adds an additional pattern107 having projections "a" and "d" different from each other corresponding to the widths W1 and W2 of both sides of the pattern 101 to be modified. Although the amount of the modification at the shorter side is not excessive in the previously proposed technique, the calculation of the projections for the both sides causes a problem in that a long period of time is required for obtaining the projections.

Accordingly, a method for use in correcting the photo-contiguous effect is desired in which a more appropriate amount of modification is possible, any increase of the period of time for modifying a pattern is not so large, and the modification can be applied only to required nodes.

Features of a method for correcting a photo-contiguous effect during the manufacture of a semiconductor device to be described below by way of example in illustration of the invention are that it does not significantly

increase the period of time required for modifying a pattern, that it provides an amount of modification which is appropriate, and that the modification is applied only to required nodes.

A method to be described below by way of example in illustration of the invention for correcting a photo-contiguous effect during the manufacture of a semiconductor device includes the steps of designating a first region specified by a first mask pattern of a first level mask, finding at least one corner from a second mask pattern in a second level mask belonging to the first region as viewed perpendicularly with respect to both the masks, locating a second region for surrounding the corner, and correcting the first mask pattern by adding the second region to the first region to form a corrected first mask pattern in the first level mask.

In a method for correcting the photo-contiguous effect to be described below by way of example in illustration of the present invention, since no correction to the second layer is carried-out where the first layer does not exist, any increase of the data and of the period of time for correcting the photo-contiguous effect can be minimised. Additionally, any deterioration of the resolution can be kept to a minimum.

Arrangements illustrative of the invention will now be described by way of example with reference to Figs. 4 to 9 of the accompanying drawings, in which:-

Fig. 4 is a schematic top plan view for use in describing a method for correcting the photo-contiguous effect during the manufacture of the

semiconductor device,

Fig. 5 is a schematic top plan view for use in describing another correction method,

Fig. 6 is a schematic top plan view showing a layout of patterns to which the method of Fig. 5 may be applied,

Fig. 7 is a schematic top plan view for use in describing yet another correction method,

Fig. 8 is a schematic top plan view for use in describing yet a further correction method, and

Fig. 9 is a schematic top plan view for use in describing a still further correction method.

With reference to Figs. 4 to 9 of the accompanying drawings, techniques of preparing data for depicting a mask utilizing an interconnect pattern obtained by modifying a pre-modified interconnect pattern in layout data will be described.

At first, terms used herein will be briefly described for the purpose of enabling a clear understanding to be made and are not restrictive upon the scope of the protection sought by the claims.

A first layer may be a square or circular connection layer such as a plug layer and a via hole layer. A second layer may be a longer connection layer such as a gate layer and an interconnect layer. The plug layer and the via hole layer are electrically connected to the gate layer and the interconnect layer.

A first peripheral region may be that partially surrounding and in contact with the first layer in addition to a circular region wholly surrounding the first layer. Corners may be formed in the shape of an arc in addition to right angled inwardly bent lines.

A second peripheral region may be formed as a plurality of divided regions corresponding to a plurality of the corners or as a single region surrounding the plurality of the corners.

In Fig.4 there is indicated diagrammatically a computer 66 which stores layout data before modification. The layout data includes an interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16, which are separated by a respective distance "c" from specified linear sides 13 and 14 which are parallel to each other, are formed by the computer 66.

The computer 66 locates a first and a second corner 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 with projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step.

The standard side 19 of the rectangular interconnect 11 is arranged to be perpendicular to the adjacent sides 21 and 22.

The first and the second additional regions 23 and 24 are surrounded by first and second shorter side common lines 25 and 26 sharing the node of the standard line 19, first and second longer side common lines 27 and 28 sharing the node of the adjacent sides 21 and 22, first and second shorter side contour lines 29 and 31 parallel to the first and second shorter side common lines 25 and 26 with a distance "a" therebetween, first and second longer side contour lines 32 and 33 parallel to the first and second longer side common lines 27 and 28 with a distance "a" therebetween, and first and second both end lines 34, 35, 36 and 37.

The first and the second end lines 34 and 36 are perpendicular to the standard line 19, and the other end lines 35 and 37 are perpendicular to the first and second longer side common lines 27 and 28, respectively. In other words, the first and the second additional regions 23 and 24 have right angled inwardly bent portions in contact with the first and the second corners 17 and 18 for surrounding the corners, respectively.

The computer 66 regards the first and the second additional regions 23 and 24 as additional interconnect nodes in a fifth step, and adds the additional interconnect nodes to the interconnect 11 for forming an additional interconnect pattern which is then stored in a post-modified layout data storing node (not shown) in the computer 66. The computer 66 formulates data for depicting a mask from the additional interconnect pattern in a sixth

step.

In Fig. 5, an interconnect structure which is a component of an interconnect pattern to be modified includes an interconnect 11a and a plug interconnect 11b. A square region of a plug 12 is included in the region of the plug interconnect 11b. Since the projection of the interconnect 11a is smaller than the projection of the plug interconnect 11b, a third corner 41 is formed in addition to first and second corners 17a and 18a. A first additional region 23a corresponding to the first corner 17a and a second additional region 24a corresponding to the second corner 18a are formed in steps similar to the first to the fourth steps of the arrangement described with reference to Fig. 4.

The computer 66 regards the first and the second additional regions 23a and 24a as additional interconnect nodes in a fifth step, and adds the additional interconnect nodes to the interconnect 11b for forming an additional interconnect pattern which is then stored in a post-modified layout data storing node (not shown) in the computer 66. The computer 66 formulates data for depicting a mask from the additional interconnect pattern in a sixth step.

An additional region 42 corresponding to the third corner 41 is also formed in steps similar to the first to the fourth steps. Data for depicting a mask corresponding to the third corner 41 is also formed in steps similar to the fifth and the sixth steps. In this manner, the interconnect 11b complying with an original design is transferred and formed by the reduction of the

three additional interconnect regions surrounding the three corners by means of the photo-contiguous effect.

Since the above-described first step in which the region separated from the parallel specified linear sides by the distance "c" is formed in the computer, and the above-described second step, in which the computer locates the plurality of the corners of the interconnect included in the above region, are conducted only to the corners in a rectangular contour region 44 having a projection "c" which surrounds the square plug for correcting the photo-contiguous effect, the correction therefor is not carried out on a plurality of corners 43 of the interconnect having no plugs as shown in Fig.6. In this manner, any increase in the size of the manufacturing data can be minimised.

In Fig. 7 there is shown a rectangular contour region 44 surrounding a plug 12 which is formed in a similar way by the computer 66. A step for locating corners 17 and 18 in the rectangular contour region 44 is similar to the above described second step. The arrangement of Fig. 7 is different from the previously described arrangements in that an additional region 51 surrounding the corners 17 and 18 is a single element.

The additional region 51 includes a single shorter side additional region 52 and longer side additional regions 53 in contact with the two sides of the shorter side additional region 52. The shorter side additional region 52 and the longer side additional regions 53 have the same length of the projections "a".

The computer 66 regards the single additional region 51 as an additional interconnect node in a fifth step, and adds the additional interconnect node to the interconnect 11 for forming an additional interconnect pattern which is then stored in a post- modified layout data storing node in the computer 66 The computer 66 formulates data for depicting a mask from the additional interconnect pattern in a sixth step.

In Fig. 8 the arrangement shown is substantially the same as the arrangement of Fig. 6, except that a projection "a" of a single longer side additional region 53a of a single additional region 54, which is substantially the same as the projection "a" of the Fig. 6 arrangement, is smaller than a projection "b" of a single shorter side additional region 52a. The projections "a" and "b" are determined in accordance with degrees of reduction of lengths due to the photo-contiguous effect which are influenced by the density of patterns and the distance between scattered nodes.

A method of reducing a problem arising from the high density of the patterns will be described with reference to Fig. 9. In this arrangement, the standard side and the adjacent sides described in the arrangement of Fig. 4 are referred to as a shorter side and a longer side, respectively. A distance "D" between adjacent longer sides of interconnects 11 and a distance "D" between adjacent shorter sides of interconnects 11 before correction are substantially the same, and are designed to have a minimum value.

A projection "d" of a single shorter side. additional region 52a is smaller than a projection "a" of a longer side additional region 53a. Accordingly, a projection "S1" between the adjacent shorter side additional regions after the correction is broader than a projection "S2" between the adjacent longer side

additional regions after the correction. By adjusting the distance between the regions in this manner, the deterioration of the resolution of the shorter side space of the pattern compared with that of the longer side space can be kept to a minimum. The unification of the additional regions does not increase the period of time for correcting the pattern without obtaining the respective length values of the additional pattern because projections of the respective sides of the additional pattern are changed.

It will be understood that although particular arrangements have been described by way of example with reference to the accompanying drawings, variations and modifications thereof, as well as other arrangements may be conceived within the scope of the appended claims.

CLAIMS

1. A method for use in manufacturing a semiconductor device which includes the steps of designating a first peripheral region specified by a first mask pattern of a first level mask, identifying at least one corner of a second layer from a second mask pattern in a second level mask belonging to the first peripheral region as viewed perpendicularly with respect to both the first and second level masks, locating a second peripheral region for surrounding the corner, and correcting the first mask pattern by adding the second peripheral region to the first peripheral region to form a corrected first mask pattern in the first level mask for correcting a photo-contiguous effect.

2. A method as claimed in claim 1 wherein the first layer is a first electrical connection layer, and the second layer is a second electrical connection layer.

3. A method as claimed as in claim 2 wherein the first electrical connection layer is a plug layer, and the second and electrical connection layer is an interconnect layer.

4. The method as claimed in claim 2 wherein the first electrical connection layer is a plug layer, and the second electrical connection layer is a gate layer.

5. A method as claimed in claim 1 wherein the first peripheral region is

a circular region surrounding the first layer.

6. A method as claimed in claim 1 wherein when a plurality of the corners exist at an end of the second layer, the second peripheral region is formed as a plurality of regions corresponding to the respective corners.

7. A method as claimed in claim 1 wherein when a plurality of the corners exist at an end of the second layer, the second peripheral region is formed as a single region surrounding a plurality of corners.

8. A method as claimed in claim 1 wherein the second peripheral region includes a shorter side addition region parallel to a shorter terminal side of the second layer and a longer side additional region adjacent to the shorter terminal side, and a projection "d" of the shorter side additional region which is different from a projection "a" of the longer side additional region.

9. A method as claimed in claim 8 wherein the projection "d" is smaller than the projection "a".

10. A method as claimed in claim 9 wherein when a plurality of the corners exist at an end of the second layer, the second peripheral region is formed as a single region surrounding the plurality of the corners.

11. A method for use in manufacturing a semiconductor device as claimed in claim 1 substantially as described herein with reference to any one of Figs. 4 to 9 of the accompanying drawings.

12. A semiconductor device made by a method as claimed in any one of the preceding claims.

The Patent Office

INVESTOR IN PEOPLE

15

Application No:	GB 9927301.3	**Examiner:**	Carol Davies
Claims searched:	1-12	**Date of search:**	30 March 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): G2X (XNB)

Int Cl (Ed.7): G03F 1/14

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	WO 97/45772 A1	(MICROUNITY) See Figures 5A, 5B	
A	US 5804339	(KIM) See Figures 2-5	
A	US 5208124	(SPORON-FIEDLER)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than the filing date of this application.